NCP4302

Secondary Side Synchronous Flyback Controller

The NCP4302 is a full featured controller and driver that provide all the control and protection functions necessary for implementing a synchronous rectifier operation in a flyback converter. With the use of the NCP4302, the space conscious flyback applications such as Adaptors, chargers, set top boxes can achieve significant efficiency improvements at minimal extra cost. In addition to the synchronous rectifier control, the IC incorporates an accurate TL431 type shunt regulator, current monitoring circuit and optocoupler driver to provide a single IC secondary solution. The NCP4302 works with any type of flyback topology (continuous mode, Quasi−resonant mode or discontinuous mode) – providing a high level of versatility.

Features

- Self−contained Control of Synchronous Rectifier in CCM, DCM, and QR Flyback Applications
- Interface to External Signal for CCM Mode
- True Secondary Zero Current Detection
- High Gate Drive Currents (2.5 A Source/Sink)
- High Voltage Operation
- Current Sense Flexibility (MOSFET $R_{DS(on)}$ OR CS Resistor)
- Accurate Low Voltage Reference
  - NCP4302A 2.55 V, 1%
  - NCP4302B 1.275 V, 1%
- Programmable Independent Secondary Side t_{on} and t_{off} Delays
- Maximum Frequency of Operation up to 250 kHz
- These are Pb−Free Devices

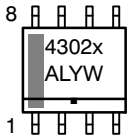
Typical Applications

- Notebook Adapters
- LCD TV Adapters
- Consumer Appliances such as DVD, VCR
- Power Over Ethernet Applications (IP phones, Wireless Access Points)
- Battery Chargers

ON Semiconductor®

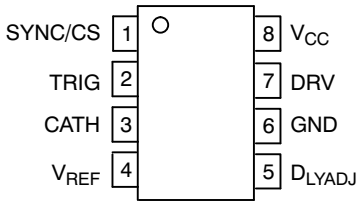
MARKING DIAGRAM

SO−8
D SUFFIX
CASE 751



x	= Reference Voltage (A or B)
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP4302ADR2G	SO−8 (Pb−Free)	2500/Tape & Reel
NCP4302BDR2G	SO−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Publication Order Number:
NCP4302/D

PIN DESCRIPTION

Pin Number	Symbol	Description
1	SYNC/CS	Connected to the flyback winding. The current on this pin is sensed and used to turn on the Synchronous Rectification MOSFET (SRFET). This pin is also used to sense the zero crossing of the MOSFET current either using the $R_{DS(on)}$ of the SRFET or using an external current sense resistor connected between drain of the SRFET and the flyback winding.
2	TRIG	Input pin for direct turn−off of the MOSFET. Typically connected to a signal from primary controller (for CCM mode) or a signal derived from the transformer (for QR mode). Has very short propagation delay to output (<50 ns).
3	CATH	Feedback compensation pin for the TL431 shunt regulator. Has the capability to sinking 10 ma of opto current.
4	V_{REF}	Output voltage feedback through resistive divider connected to this pin. Regulated at 1.28 V (option B) or 2.55 V (option A).
5	D_{LYADJ}	A resistive divider between the power supply output and ground with the center point tied to the D_{LYADJ} input pin allows for independent adjustment of the minimum t_{on} and t_{off} delay time. The maximum external capacitance from this pin to ground is 25 pF.
6	GND	Return pin for the controller − connected to the output return.
7	DRV	Drive output for external MOSFET − 2.5 A peak drive capability, internally clamped to 13.5 V (Maximum)
8	V_{CC}	Bias voltage for the controller. Maximum voltage is 28 V.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Current	V_{CC} I_{CC}	−0.3 to 28 100	V mA
Drive Voltage Current	V_{DRV}	−0.3 to 18 100	V mA
Drive Current Source Sink	I_{DRV}	 2.5 −2.5	Apk
Analog and Logic Inputs	TRIG, V_{REF}, D_{LYADJ}	−0.3 to 10 100	V mA
Maximum Voltage Current	SYNC/CS	− 10 to 95 100	V mA
Operating Junction Temperature Range	T_J	−40 to 125	°C
Maximum Junction Temperature	T_{Jmax}	150	°C
Storage Temperature Range	T_{Smax}	−65 to 150	°C
Lead Temperature (Soldering, 10 s)	T_{Lmax}	300	°C
Reference input Current, continuous	I_{REF}	−0.05 to 10	mA
Total Power Dissipation	P_D	225	mW
Thermal Resistance Junction−to−Ambient	θ_{JA}	178	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Pin 1−8: Human Body Model 2000 V per Mil−Std−883, Method 3015.
   Machine Model Method 200 V
2. This device contains Latch−up protection and exceeds ±100 ma per JEDEC Standard JESD78

ELECTRICAL CHARACTERISTICS

(V_{CC} = 19 V, Sync frequency = 100 kHz, V_{REF} = V_{KA} (I_{KA} = 1 mA), R_S = 75 ohms, V_{TRIG} = GND, C_{DRV} = 1 nF, R_{DLYADJ} = 30.1 k, V_{DLYADJ} = 2.0 V, for typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, unless otherwise noted)

Rating	Test Conditions	Symbol	Min	Typ	Max	Unit
V_{CC}						
Start−up Threshold	V_{CC} ↑, SYNC/CS = 0 to −0.5 V 100 kHz, 5 μs pulse, Trig = 0 V	$V_{CC(on)}$	9.6	10.4	11.2	V
Stop Threshold	V_{CC} ↓, SYNC/CS = 0 to −0.5 V 100 kHz, 5 μs pulse, Trig = 0 V	$V_{CC(off)}$	8.5	9.2	−	V
V_{CC} shutdown Hysteresis	$V_{CC(on)}$ − $V_{CC(off)}$	$V_{CC(HYS)}$	0.9	1.2	1.4	V
Supply current after turn−on	no−load on DRV pin, SYNC/CS = 0 to −0.5 V 100 kHz, 5 μs pulse, Trig = 0 V	I_{CC1}	−	2.7	5.6	mA
Supply current after turn−on	SYNC/CS = 0 to −0.5 V 100 kHz, 5 μs pulse, Trig = 0 V	I_{CC2}	−	3.6	7.5	mA
DRIVE OUTPUT						
Output voltage rise−time	10−90% of the output signal SYNC/CS = 0 to −0.5 V 100 kHz, 5 μs pulse, Trig = 0 V	t_r	−	−	40	ns
Output voltage fall−time	10−90% of the output signal SYNC/CS = 0 to −0.5 V, 100 kHz, 5 μs pulse, Trig = 0 V	t_f	−	−	40	ns
Output source current (Note 3)		$I_{DRV(source)}$	−	2.5	−	Apk
Driver high level output voltage	I_{SOURCE} = 200 mA, SYNC/CS = 0 to −0.5 V 100 kHz, 5 μs pulse, Trig = 0 V, V_{CC} = 12 V	$V_{DRV(H)}$	6.5	9.5	−	V
Output sink current (Note 3)		$I_{DRV(sink)}$	−	2.5	−	Apk
Driver Output low level output voltage	I_{SINK} = 200 mA, SYNC/CS = 0 to −0.5 V 100 kHz, 5 μs pulse, Trig = 0 V, V_{CC} = 12 V	$V_{DRV(L)}$	−	160	500	mV
Drive voltage internal clamp	V_{CC} = 28 V, SYNC/CS = 0 to −0.5 V 100 kHz, 5 μs pulse, Trig = 0 V, DRVpin = 10 kΩ	$V_{DRV(CLMP)}$	−	−	17	V
Minimum drive output voltage	V_{CC} = $V_{CC(off)}$ + 200 mV, DRV pin = 10 kΩ + 1 nF, SYNC/CS = 0 to −0.5 V 100 kHz, 5 μs pulse, Trig = 0 V	$V_{DRV(MIN)}$	5.5	6.5	−	V
SYNC/CS						
The total propagation delay from SYNC/CS to the DRV output	SYNC/CS = +0.5 V to −0.5 V 100 kHz, 5 μs pulse, (Trig = 0 V)(Refer to the Drive Output specifications for Tr 50% of the output signal	t_{p1}	−	70	135	ns
Zero Current Detection	$V_{SYNC/CS}$ < −30 mV	Is(zcd)	50	230	450	μA
Current Sense Pin Offset Voltage at Zero Current Level (Note 3)		VS(ZCD)	−30	−	−	mV
SYNC/CS Leakage current	$V_{SYNC/CS}$ = 95 V	$SCS_{Leakage}$	−	−	10	μA
TRIGGER SECTION						
Minimum Trigger pulse duration	SYNC/CS = 0 to −0.5 V 100 kHz, 5 μs pulse, Trig ↑	trig−pw	75	−	−	ns

3. Guaranteed by Design

ELECTRICAL CHARACTERISTICS

(V_{CC} = 19 V, Sync frequency = 100 kHz, V_{REF} = V_{KA} (I_{KA} = 1 mA), R_S = 75 ohms, V_{TRIG} = GND, C_{DRV} = 1 nF, R_{DLYADJ} = 30.1 k, V_{DLYADJ} = 2.0 V, for typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, unless otherwise noted)

Rating	Test Conditions	Symbol	Min	Typ	Max	Unit
TRIGGER SECTION						
Trigger Pulse Voltage for Gate turn−off	SYNC/CS = 0 to −0.5 V 100 kHz, 5 μs pulse, Trig ↑	Vtrig	2.0	−	4.0	V
Propagation delay from TRIG to DRV turn−off	C_{DRV} = no−load, SYNC/CS= −0.5 V 100 kHz, 5 μs pulse, Trig = 0−5 V ↑	t_{p2}	−	25	85	ns
TL431 CHARACTERISTICS						
Reference input voltage	I_{KA} = 5 mA, V_{KA} = V_{REF} NCP4302A T_J = +25°C T_J = −40°C to +125°C	V_{REF}	 2.525 2.499	 2.55 −	 2.575 2.60	V
Reference input voltage	(I_K = 5 mA, V_{KA} = V_{REF}) NCP4302B T_J = +25°C T_J = −40°C to +125°C	V_{REF}	 1.262 1.249	 1.275 −	 1.288 1.301	V
Reference Input Current	I_{KA}= 10 mA	I_{Ref}	−	0.0018	4.0	μA
Minimum CATH current for regulation	I_{SOURCE} ↑ 0 to 1 mA	I_{KA}	−	0.5	1.0	mA
Reference voltage line regulation	ΔV_{KA} = V_{CCon}− 16 V, I_{KA} = 1 mA $= \frac{\Delta V_{REF}}{\Delta V_{KA}}$	V_{KA}	−	2.0	5.0	mV/V
Off−State CATH Current	V_{KA} = 18 V, V_{REF} = 0 V (test circuit 2, V_{REF} pin grounded)	I_{Off}	−	11	20	μA
Dynamic impedance	V_{KA} = V_{REF}, ΔI_{KA} = 1 mA to 10 mA	Z_{KA}	−	0.62	1.5	Ω
The maximum sink current capability	(I_{SOURCE} ↑ 0 to 10 mA)	Isinkmax	10	−	−	mA
ADJUSTABLE TIME DELAY						
The t_{on} time delay	SYNC/CS = 0 to −0.5 V 100 kHz, 5 μs pulse, Trig = 0 V CD_{LYADJ} internal = 10 pF (Vs = 2.0 V, Rth = 30.1 kΩ)	$t_{on(delay)}$	1.0	1.4	1.8	μs
The min and max $t_{on(delay)}$ range (Note 3)	* R2 = 190 kΩ, R3 = 57 kΩ * R2 = 499 kΩ, R3 = 39 kΩ (*See Figure 27)	$t_{on(range)}$	 0.45 −	 − −	 − 2.0	μs
The maximum and minimum input voltage operating range. (Note 3)	The maximum capacitance from pin 5 to ground is 25 pF.	Vin_{DLYADJ}	1.5	−	4.5	V
The maximum and minimum input operating current into the D_{LYADJ} pin (Note 3)		Iin_{DLYADJ}	9	−	200	μA
The t_{off} time delay	SYNC/CS = 0 to −0.5 V 100 kHz, 5 μs pulse, Trig = 0 V CD_{LYADJ} internal = 10 pF (Vs = 2.0 V, Rth = 30.1 k)	$t_{off(delay)}$	3.1	4.1	5.1	μs
The min and max $t_{off(delay)}$ range (Note 3)	R2 = 66 k, R3 = 23.6 k * R2 = 408 k, R3 = 32.4 k (*See the schematic below)	$t_{off(range)}$	 0.8 −	 − −	 − 4.6	μs

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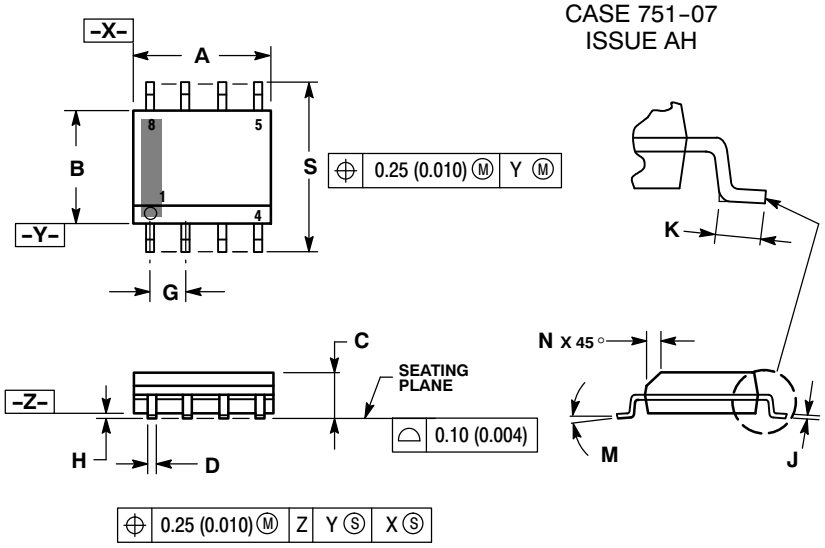
PACKAGE DIMENSIONS

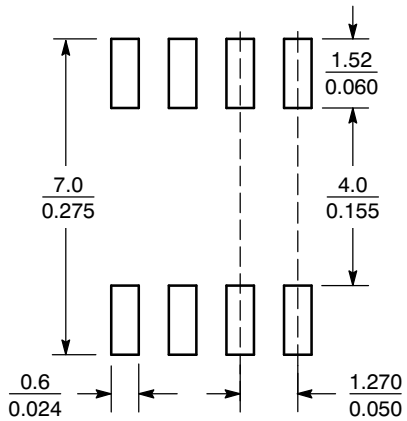
SOIC−8
NB SUFFIX
CASE 751−07
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.